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Procedia Computer Science 171 (2020) 969–978

Procedia Computer Science

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Third International Conference on Computing and Network Communications (CoCoNet'19)

Computer Aided Numerical Simulations of Current Induced Domain Wall in a Nanowire

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Abstract

This paper proposes the numerical simulations of soft modes of an magnetic domain wall induced by current in a compressed nanowire. We model the Hamiltonian of a nanowire by studying the variations of the parameters with spin-orbit coupling and axial magnetic field. We simulate the variation of chemical potential versus the density of states with spin orbit coupling energy along with Zeeman strength with respect to the energy density . Further we also study of tight binding parameter with spin-orbit coupling energy. Band structure of compressed nanowire is obtained along with simulation of three dimensional electron density and transmission and current density factors. Throughout the manuscript we investigate and make a experimental design of device physics, device characteristics and logical architecture of nanowire required to develop multiple-bit per single cell memory, utilized in high performance computing and vision systems. Using GPU accelerated Micromagnetic framework we simulate the stapled domain wall in a compressed region.

Keywords: Compressed Nanowire; Magnetic memory; Magnetic Domain Wall; Multi-Bit per Cell Memory

1. Introduction

The encoding of discrete variables in a domain wall for quantum annealing process in quantum networking which requires the optimization problem to be effectively mapped to a Hamiltonian.
In the year 2016, Sbiaa and Bahri carried out extensive research and proposed a novel technique to attach a domain wall (DW) with the appropriate orientation in a generic model of magnetic nanowire [1]. The current manuscript further extends the work by investigating the variation of parameters and modeling the generic model of the nanowire with carrying out the simulations of magnetization profile in graphics processing unit (GPU) accelerated framework. Magnetic DW exhibiting magnetic nano wires are studied extensively for magnetic memory of high density and com-

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10.1016/j.procs.2020.04.105

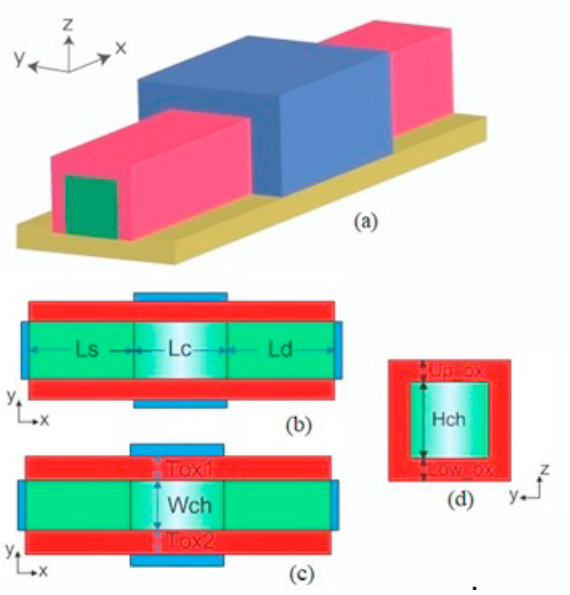

Fig. 1. (a) Schematic representations of a rectangular nanowire (b) Geometry-X (c) Geometry-Y (d) Geometry-Z

puting paradigm [2, 3, 4, 5]. This section presents the introduction along with analysis of rectangular nanowire in confined geometry in X,Y and Z-axis. The concept of physics elucidated in terms of electron spin based phenomenon is called as spintronics. The neurons and synapses which constitute the computational primitives can basically function to directly mimic the biological structures. They operate with computations at very low terminal voltages, and research works conducted very recently have depicted several verticals based on the underlying physics of spin transport and manipulation [6]. With the characteristics such as non-volatility, high access speed, and low operational power, the spin transfer magnetic random access memory (STT-MRAM) is most popular device in terms of emerging memory technology. At dimensions which are scaled, the transient and permanent failures remain as a major hurdle [7, 8]. A non-volatile domain wall memory(DWM), a physics based model, which is capable in terms of excellent density, standby power, and retention for next generation cache. The DWM characterize the process variations and Joule heating effects. The process variations can be leveraged for device authentication by building robust security primitives. In the rectangular nanowire the crystal orientation to the transport direction is at extremal corners of (1 0 0), with confinement direction in y is (0 1 0) and confinement direction in z is (0 0 1). Figure 1(a) depicts a rectangular type nanowire in which the magnetic polarization is directed along the x-axis and the current polarized with spin is flowing along the horizontal x-axis in the nanowire [9, 10, 11]. The channel length (Lc) is fixed at 15nm, the source length (Ls) and device length (Ld) is fixed at 10nm for geometry X as shown in Figure 1(a). Further in geometry Y in the Figure 1(b) the wall on the left side of the channel when looking from source to drain ie. the left wall oxide thickness(ToX1) is 1nm and similarly the right wall oxide thickness(ToX2) is also 1nm. Again in geometry Z the thickness of oxide on top of the channel denoted as upper oxide thickness and thickness of oxide beneath the channel denoted as lower oxide thickness is 1nm. We have selected the channel material as Gallium Arsenide (GaAs) with the dielectric constant of channel as 13.1 and affinity of the channel material is 4.07eV as depicted in Figure 1(a). Further the dielectric constant of the insulator and Gate contact work function is 3.9 and 4.1 eV respectively. Further as seen in Figures 1(b), (c) and (d) the bias information is obtained as total number of bias points as 13 with gate(Vg) and drain (Vd) voltages at 0.6V. In the characteristics of drain current (Id) versus gate voltage (Vg) is plotted with change of gate bias with fixed drain bias and drain bias is to be swept first fixing the gate bias [12].

The further sections of this research manuscript is organized as section 2 presents the related work with section 3 illustrate the hypothetical model of a rectangular nanowire along with indepth numerical analysis of the model. The section 4 presents experimental analysis along with detailed algorithm steps which is used to simulate the experimental results, the results are obtained by carrying the simulations in various software frameworks used such as Micromag-

netic simulation framework, Jupyter notebook of python simulation framework. The section 5 presents the lessons learnt section which provides the further directions in this research work. The conclusions are presented in section 6 followed by references at the end of the manuscript.

2. Related Work

The research interest has been intensively attracted with focusing on reliability of integrated circuits (ICs) since its origin. The functionality and performance of today's computing system are increasingly dependent on the characteristics of the memory subsystem [13]. Merging non volatile memory technologies face challenges from aspects of process compatibility, manufacturing yield, performance variability, and reliability [14]. Different emerging non volatile memory (NVM) devices may have different application spaces in the memory hierarchy due to their unique characteristics. Beyond the conventional memory applications, novel applications that use emerging NVM are arising. The reliability of microelectronics devices lies in the structural elucidation, evaluation of dynamic power consumption for a given in-memory computing implementation and mechanism study of devices based on the computing architectures [15]. Typically a storage device, which consists of multiple number of binary digits use spin electronics as a information carriers, where the device is charged by an electric current which causes the shift resulting in mobility of spin electronics candidates in and out of the device. The spin transfer torque magnetic tunnel junction (STT-MTJ)-based non-volatile memory features non volatility, infinite endurance, fast random access with an achievement in spin transfer on field induced writing [16]. The limitation identified here is in the small and complex device the magnetic writing problem arises. In SPICE compatible Magnetic Tunnel Junction(MTJ) compact models features logic-in memory architecture with fast read/write with five stage pipeline architecture [17]. This technique is not applicable to realizing ultralow- power VLSI processor. The STT-MRAM (spin-transfer torque magnetic random access memory) features switching from in plane MTJ to Perpendicular MTJ which allows better scalability and longer retention time[18]. Here the MTJ's scalability is limited by the aspect ratio (length/width in the lateral dimension) of the cell. The PCRAM (phase change random access memory) features extremely scaled carbon tube electrodes here the write current can achieve nearly 1μA at 2nm node. Here switching speed is reduced by slow crystalline process [19]. The RRRAM (Resistive random-access memory) could require smaller write current (up to 10μA) due to the filamentary switching mechanism with more switching speed [20]. The limitation is less endurance and larger write currents required in the uni-polar mode. In CBRAM (Conductive Bridging random-access memory) device the filament consists of metal atoms, formed by fast-diffusive silver (Ag) or copper (Cu) ions migrating into the solid-electrolyte[21]. This achieves the on/off resistance ratio which can be quite large (10^3 to 10^6) with limited endurance (up to 10^4 cycles).

3. Hypothetical Model

The hypothetical model of rectangular nanowire as described in Figure 1 in the introduction section is further characterized in Table 1 with the classification of magnetic parameters used in simulation of the device [22]. The domain wall position and profile of magnetization is computed for different values of time such as for t=0.22ns, t=0.31ns, t=0.42ns, t=0.7ns, the length of stepped nanowire, and the width w is as depicted in Table 1 along with the magnetic properties of the nanowire. With the above values we compute the normalized x-component of the magnetization of the nanowire for different values of offset 'd' such as d=5nm, 10nm, 15nm, 25nm, 35nm as a simulation component. The length, width and magnetic properties of the investigated material are as described in Table 1. Here we consider three cases as depicted in Table1 as thin film cuboid, one dimensional nanowire cuboid, and one dimensional domain wall. We start the analysis by studying a basic thin film cuboid whose device geometry and material parameters are as illustrated in Table 1, with the simulated sample of thin film cuboid with dimensions: - length L = 500 nm, width d = 125 nm, and thickness t = 3 nm. The dynamic processes in magnetization elucidated as magnetization dynamics is controlled by the (LLG) equation:

$$\frac{d\mathbf{S}}{dt} = \mathbf{S} \times \frac{\delta \mathcal{H}[\mathbf{S}]}{\delta \mathbf{S}} - j\frac{\partial \mathbf{S}}{\partial z} + \beta j\mathbf{S} \times \frac{\partial \mathbf{S}}{\partial z} + \alpha \mathbf{S} \times \frac{d\mathbf{S}}{dt} \tag{1}$$

Table 1. Classification of Magnetic Parameters

Type	Length	Width	Magnetic Parameters
1. Thin Film Cuboid	500 nm	125 nm	Exchange Energy A(J/m) Saturation Magnetization Ms(A/m)
2. 1-D nanowire Cuboid	1000 nm	Fixed	A(J/m),Ms(A/m), 1st order uniaxial anisotropy Ku(J/m^3)
3. 1-D Domain Wall	500 nm	-	A(J/m),Ms(A/m),K1(J/m^3), K2(J/m^3)
4. Conventional Nano wire	200 nm	-	Ms(kA/m),Ku(J/m^3),A(J/m)
5. Stepped Nano Wire	200 nm	40 nm	Ms(kA/m),Ku(J/m^3),A(J/m)

The system is initially relaxed at zero external magnetic field and then, from the obtained equlibrium configuration, the magnetization dynamics is simulated for each of two different external magnetic fields such as H1=(-24.6,4.3,0.0)mT and H2=(-35.5,-6.3,0.0)mT. Initial magnetization is obtained by ignoring the decreasing external field. The system can be relaxed and the obtained equilibrium configuration is saved, and utilized as an initial state for simulating magnetization dynamics.With the obtained relaxed magnetization, the evolution of magnetization can be simulated for the two different external magnetic fields and we obtain the average magnetization time evolution components. In this case the simulated sample is a 1D nanowire cuboid whose device geometry and material parameters are as illustrated in Table 1 for case 2. After the system is relaxed to a domain wall, with a spin-polarised current with J = 1 x $10^{12}A/m^3$ density is applied in the positive x direction in extremal corners of (1,0,0). The domain wall is at the maximum value of mz or my, consequently the domain wall position is maximum mz at x = 124. With the obtained domain wall equilibrium state, the motion is simulated in presence of a spin-polarized current [23]. We compare the initial state with the ones after a spin-polarized current is applied for component to observe the domain wall motion and compute until the system reaches nearly 5 ns to improve the effect [24]. Again, in the third case of a one-dimensional domain wall simulated sample is a 1D-domain wall. Whose device geometry and material parameters are as illustrated in Table 1 for case 3 the domain wall profile is computed for one-dimensional domain wall of L= 500 nm length. The standard values of material parameters of the simulated material are as depicted in Table 1 here the initial magnetisation is set to be in extremal corners of (0; 0; 1) direction for x ≤ 0:4Lnm, in extremal corners of (1; 0; 0) direction for 0:4Lnm ≤ x ≤ 0:6Lnm, and in extremal corners of (0; 0; 1) direction for x > 0:6Lnm. Further the magnetization is initialized, and the system is relaxed to to its equilibrium state and the magnetization profile [25].

4. Experimental Analysis and Results

This section presents the experimental results with classification of various techniques. The algorithm steps for simulation of domain wall(DW) oscillation in compressed nanowire are illustrated as follows. The algorithm is programmed in micro-magnetic simulation framework to simulate domain wall oscillation in compressed nanowire. As the algorithm was simulated the domain wall was blocked at the constricted region of d=15nm. The spin polarization of the applied current is 0.6 and damping constant is 0.014, the polarized electric current is flowing along positive x-direction. It is noteworthy that the stability of domain wall occurs after small damped oscillations [26, 27]. Jc is the critical current density, which is the maximum current density to keep the domain wall stability. For same value of d, narrower device requires larger critical current to shift the domain wall from the stepped region. Since due to the remaining space w-d, an almost linear dependence of critical current density (Jc) was observed. Here the mesh size was fixed to 2nm * 2nm * 3nm in x, y, and z-axis direction respectively. The algorithm steps to simulate domain wall oscillation in compressed nanowire in MUMAX3 to reproduce result obtained in Fig-

ure 2(a). With these steps we observed that domain wall is bound to the compressed region of the nano-wire [28].

```
Result: Domain Wall in Compressed Nanowire
Start;
Define parameters;
while Set exchange length 'L' do
    Set cell dimensions to x nm * y nm * z nm;
    Define grid size and cell size ;
    SetGridSize(Nx, Ny, Nz) ;
    SetCellSize(sizeX/Nx, sizeY/Ny, sizeZ/Nz);
    if Define geometry then
        struc1 := cuboid(A, B, C).transl(A, B, C);
        struc2 := cuboid(A1, B1, C1).transl(A1, B1, C1);
        struc := struc1.add(struc2);
        setgeometry(struc);
    else
        Compute the regions;
        defregion(1,struc) and save Regions;
        Material Parameters: (set up free layer);
    end
    Compute;
    Ms(kA/m);
    Ku(J/m^3);
    A(J/m);
    LLG Constant α;
    Define Initial Reduced Magnetization;
    Set runtime;
    Initialize excitation;
    compute current density vector;
    compute Electrical current polarization;
    save vector and data field ;
    save simulations;
end
```

Algorithm 1: Algorithm steps to simulate domain wall(DW) oscillation

Further we also calculate the Hamiltonian in Figure 2(b) and density of states in Figure 2(c) using axial magnetic field and with spin-orbit coupling with the parameters as illustrated in the following

- Number of points in z direction,
- Tight binding parameter,
- Chemical potential which is assumed to be same across the device,
- Spin-orbit coupling energy and Zeeman strength.

The Figure 2(a) elucidates the view of simulation result of magnetic nanostructures as domain wall nanowire is under study and obtained in mumax3 which is the open source GPU accelerated micro magnetic simulation program which offers the performance acceleration systems with graphic processing units. Micromagnetic simulation is performed with Mumax 3.9.1c (CUDA 9020 GeForce GTX 1050). Further the study of variation with chemical potential, Zeeman strength (Vx) with respect to the energy density(E),(a tight binding parameter with spin-orbit coupling energy) are plotted in Figures 3(a), (b) and (c) respectively. Again the analysis of the band structure of the compressed nanowire is performed and the band structure is considered to be a tight binding model without spin-orbit coupling energy [29]. The Figure 4 depicts the band structure of compressed nanowire with number of modes as 16 and number of K points as 101. Further a one dimensional band structure for a drain voltage Vd=0.6 Volts is as depicted in Figure 5 and is characterized with the plot with energy density in electrons volts(eV) versus the length of the nanowire in x-nm.

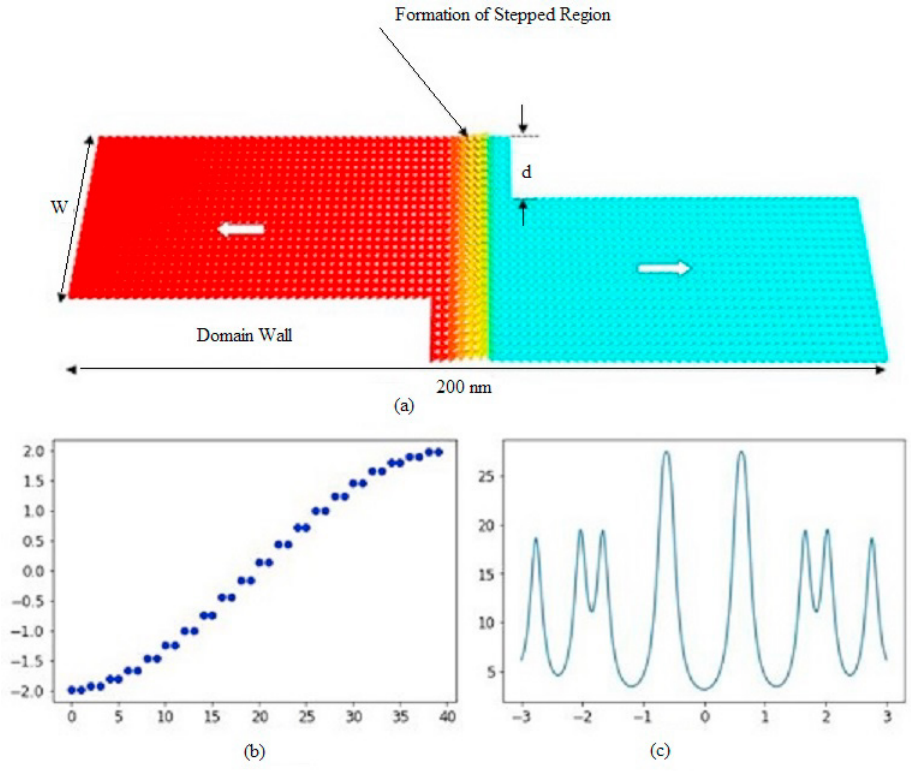

Fig. 2. (a) Magnetization profile of magnetic nanostructure (b) Hamiltonian Plot (c) Density of states plot

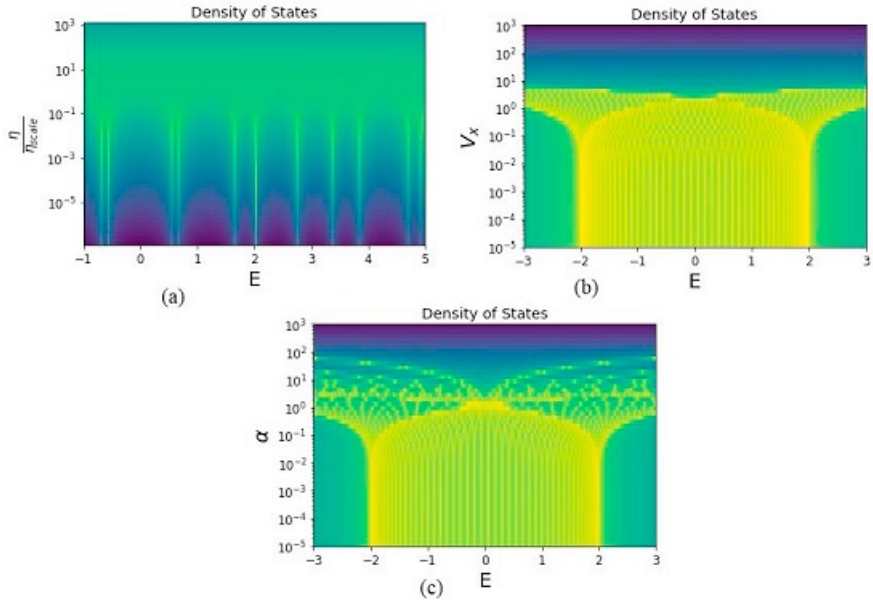

Fig. 3. (a) Study of variation of chemical potential versus the density of states with spin orbit coupling energy (E) (b) Zeeman strength (Vx) with respect to the energy density (E) (c) Study of tight binding parameter with spin-orbit coupling energy.

Fig. 4. Band structure of compressed nanowire

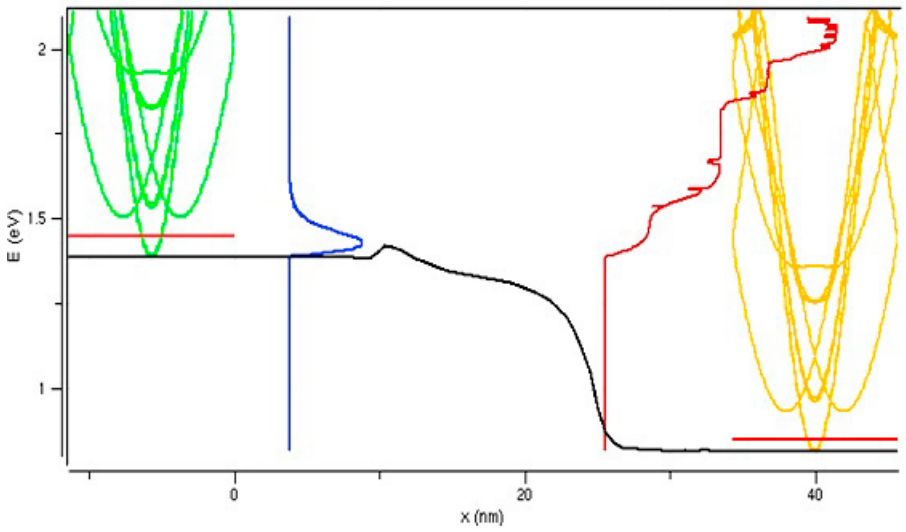

Fig. 5. one dimensional band structure for a drain voltage Vd=0.6 Volts

The simulation of a three dimensional electron density for the drain voltage of Vdd=0.6Volts and gate voltage Vg=0.6 V is carried out and is as illustrated in Figure 6(a). Further as the gate voltage Vg is varied to 0.2 Volts maintaining the drain voltage to Vd to 0.6 Volts , the change in the 3-Dimensional electron density is calculated. In the Figure 6(b) the electron density is at drain voltage Vd=0.6 Volts and gate voltage Vg is at 0.2 Volts. Further the three dimensional electro-static potential is obtained as illustrated in Figure 6(c) where the gate voltage is set at 0.25 Volts and drain voltage is again set at 0.6 Volts. At the end we present the transmission and the current density factor for the drain voltage 0.6 Volts and gate voltage set to 0 Volts, which is shown in Figure 7 where the current density factor is normalized [30].

5. Lessons Learnt

This section discusses the lessons learnt in this research which aims towards the insight into the further directions of this research work. The Figure 8 illustrates a comprehensive summary of the material parameters used in simulated material and to carry out the simulation of the magnetization profile of the magnetic nanostructure as depicted in the algorithm 1 as elucidated under experimental analysis. The new devices, new architectures which are with or without new devices and new paradigms of computation form to be a basic roadmap for new directions in comput-

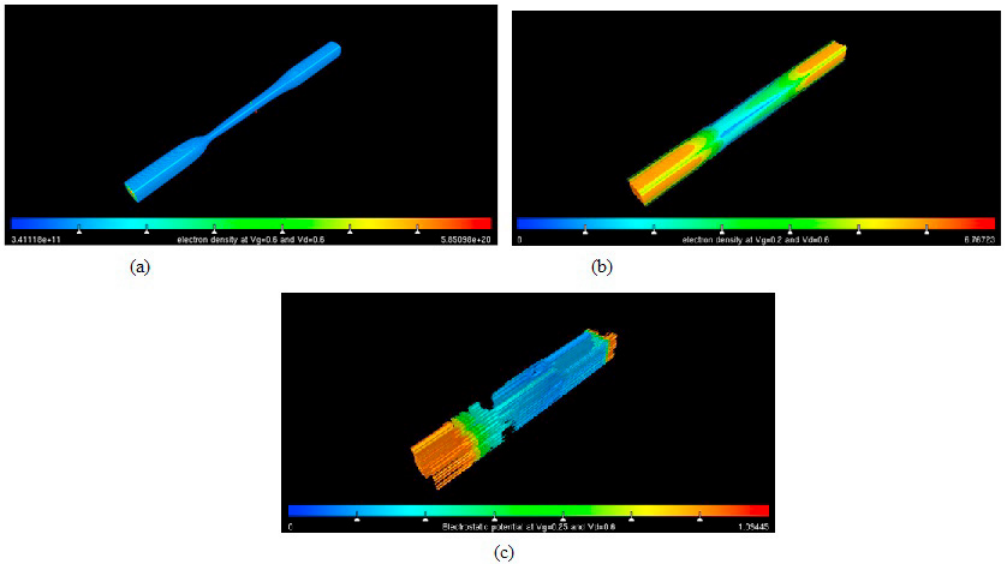

Fig. 6. (a) Simulation of a three dimensional electron density (b) The electron density is at drain voltage Vd=0.6 Volts and gate voltage Vg at 0.2 Volts (c) Three dimensional electro-static potential

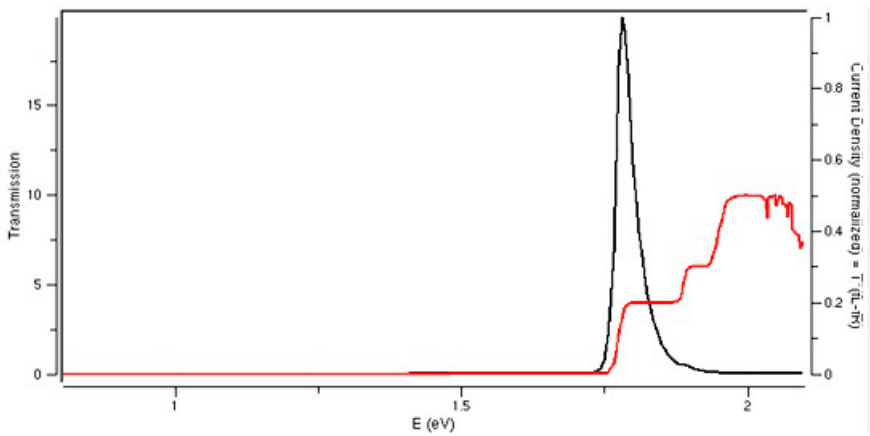

Fig. 7. Transmission and the Current density factor

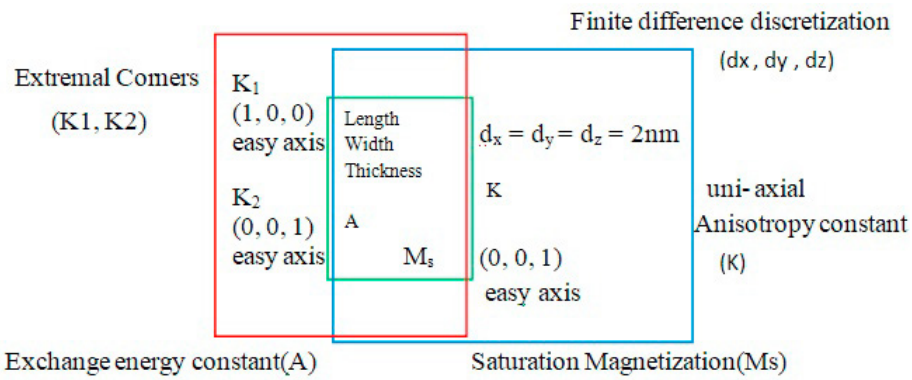

Fig. 8. Summary model of material parameters used in simulated material

ing. One of the research needs of Beyond CMOS emerging computer architecture is neuromorphic computing. The aim of this requirement is to evaluate research opportunities available with advanced materials, scientific computing, and bio-inspired computing architectures[31]. The spintronics based magnetic interactions along with charge-based devices as well as biological devices help in the physical realization of the computing devices and characteristics of In-memory, nanotechnology computing devices are more stochastic in nature [32]. The algorithm techniques are tightly linked with processor architecture techniques, with memory bottleneck and processor bottleneck discussed to increase efficiency and enable the inference of deep neural networks in hardware devices along with an initiative to develop a hardware-algorithm cooptimization method. To develop the fault-tolerant algorithms to which the approximate computing techniques can be applied. Further one of the lesson learnt is the dynamic range of highly accurate computations of necessary precision must be supported in any modern approximate computing technique. In paradox of programming a neuromorphic computer. It is learnt that we need to figure out the new class of algorithms, we are also missing out some very important basic concepts. Algorithms create input-output mappings using rules or weights stored in memory, are created by humans. Biological memory corresponds to a container holding data and algorithms. The complete timeline of building a intelligent computational system starts designing a boolean logic or functions, passes through theory of computation phase, next enters into electronics technology phase, and further into computational complexity phase and ends at a practical computation phase. The lesson learnt here is while dealing with intelligence in the first stage is to probe into evolution, complexity, and also thermodynamics which is not an equivalent of a boolean logic or functions, and during the second stage new and novel electronics technology [33] is required which is not an equivalent of elctronics technology, which was defined during the computation phase, in the further in third stage the implementation complexity is not an equivalent to computational complexity, and the final stage is the practical intelligence stage which is also not an equivalent practical computation stage, defined during process of computation. In all of these intelligence and computation phases the lesson learnt is that the concept of physics is missing [34]. Multi-level mapping of hardware-based silicon-computer architectures dealing with the issue of mapping large applications to hierarchical architectures built with emerging nanoscale devices. The convergence of intellectual property re-use and multi-level mapping theories explores the ”O-cycle” design process into the corresponding mapping framework which is versatile and time-efficient in terms of circuit design. With this resultant mapping technique, there is a significant improvement in power and delay parameters for specific circuit architectures. This demonstrates the efficient allocation of energy, the critical delay path and the die-area. Reconfigurable VLSI architecture illustrates a versatile nano-electronic system design by exploring the concept of reconfigurable computing by applying the principles of moving target defense to dynamically reconfigure the logic framework to make it a more secure network. The potential scope of this research work elucidates the method of reconfigurable reversible computing-based cryptography and the re-configuration of a general design-for-security solution. In the future, both approaches would be evaluated through case studies using a high-speed, high-performance embedded processor.

6. Conclusion and Future Scope

In this manuscript we have implemented the oscillation of stabilized magnetic domain wall in compressed nanowire, through a novel method of accurately binding domain wall in a desirable position and is stabilized precisely by using a stepped nanowire. In order to enable the reliability of future nanowire based spintronics devices, the domain wall motion of magnetic nanowires must be completely illuminated. For optimization problem to be effectively mapped to a Hamiltonian the requirement is the encoding of discrete variables in a domain wall for quantum annealing process in quantum networking. This fundamental work paves a way for development of novel skyrmion based spintronics devices and high dimensional memory architectures.

Acknowledgements

The authors would like to thank the reviewers for the detailed reviews and constructive comments, which have helped improve the quality of this paper. This work is supported by the Research Assistantship offered by School of Electronics and Communication Engineering, REVA University, Bengaluru, India.

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